

Serial No. 10/725,325

CLAIM AMENDMENTS:

Please cancel Claim 24.

Please amend Claims 18, 19, 25 and 27 as shown.

1-17. (Canceled)

18. (Currently Amended): A method of forming a trench MOSFET device comprising:

providing a substrate of a first conductivity type;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending to a greater depth from said upper surface of said epitaxial layer than does said body region;

forming a doped region of said first conductivity type between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer,

wherein said doped region is diffused and spans 100% of the distance from said trench bottom portion to said substrate, and

wherein the steps of etching said trench and forming said doped region comprise: (a) forming a trench mask on said epitaxial layer; (b) etching said trench through said trench mask; (c) implanting a dopant of said first conductivity type through said trench mask; and (c) diffusing said dopant of said first conductivity type at elevated temperature;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer; and

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench.

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Serial No. 10/725,325

19. (Currently Amended) The method of claim 18, wherein said step of forming said doped region comprises: (a) implanting a dopant of said first conductivity type into said epitaxial ~~region~~ layer; and (b) diffusing said dopant of said first conductivity type at elevated temperature.

20. (Canceled)

21. (Canceled)

22. (Original) The method of claim 19, wherein said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

23. (Original) The method of claim 22, wherein said dopant is phosphorous.

24. (Canceled)

25. (Currently Amended) A method of forming a trench MOSFET device comprising:

providing a substrate of a first conductivity type;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending to a greater depth from said upper surface of said epitaxial layer than does said body region;

forming a doped region of said first conductivity type between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer,

Serial No. 10/725,325

wherein the steps of etching said trench and forming said doped region comprise: (a) forming a trench mask on said epitaxial layer; (b) etching said trench through said trench mask; (c) implanting a dopant of said first conductivity type through said trench mask; and ~~(e)~~ (d) diffusing said dopant of said first conductivity type at elevated temperature; forming an insulating layer lining at least a portion of said trench; forming a conductive region within said trench adjacent said insulating layer; and forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench,

wherein said elevated temperature is provided by a step in which a sacrificial oxide is grown along walls of said trench.

26. (Original): The method of claim 18, wherein said trench MOSFET device is a silicon device.

27. (Currently Amended): The method of claim 18, further comprising: forming a metallic drain contact adjacent said ~~semiconductor~~ substrate, forming a metallic source contact adjacent an upper surface of said source region, and forming a metallic gate contact adjacent an upper surface of said conductive region remote from said source region.